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Novel Design of Low Power Comparator Using Reversible Gates

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Abstract:- Reversible logic has shown potential to have extensive applications in emerging technologies such as quantum computing, optical computing, quantum dot cellular automata as well as ultra low power VLSI circuits. The classical logic gates such as AND, OR, EXOR and EXNOR are not reversible. In the existing literature, reversible sequential circuits designs are offered that are improved for the number of the garbage outputs and reversible gates. Minimizing the number of garbage is very noticeable. This paper presents a novel design of reversible comparator using the existing reversible gates and proposed new Reversible BJN gate. All the comparators have been modeled and verified using VHDL and ModelSim. A comparative result is presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost. The design is useful for the future computing techniques like quantum computers. The proposed designs are implemented using VHDL and functionally investigated using Quartus II simulator.

Keywords – Advanced computing, Modified Toffoli gate, Reversible arithmetic unit, Reversible logic circuits.

1. INTRODUCTION

Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation [1]. According to Landauer's principle, each bit of data lost produces kTln2 joules amount of heat, where k is Boltzmann's constant and T is the absolute temperature at which the operation is implemented [2]. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs but also the inputs can be uniquely recovered from the outputs. Additional inputs or outputs are added so that the numbers of inputs are made equal to the number of outputs whenever it is necessary. An important constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed.

A reversible circuit should be designed using minimum number of reversible gates. One key requirement to achieve optimization is that the designed circuit must produce minimum number of garbage outputs, also they must use minimum number of constant inputs [3, 4].The reversible comparator proposed in this paper is designed with an idea of retaining two of the three outputs Considering any one of them redundant. This novel idea optimizes the design in terms of gate count, garbage output, constant input and quantum cost. The present paper proposes several alternate designs of a comparator circuit using existing reversible logic gates. The Present paper proposes a new gate, called Reversible BJN gate which is used in the design of comparator along with the existing Reversible gates. This work proposes various comparator designs and compared for their performance parameters.

All the proposed designs are virtually implemented using VHDL and functionally verified using ModelSim simulator. In this paper, we present various designs of a three-bit comparator circuit using existing reversible

logic gates. The present paper proposed a new gate, called reversible DG gate which was used in the design of comparator.

2. BASIC REVERSIBLE LOGIC GATES

2.1 Reversible logic: The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design , optical computing, quantum computing and nanotechnology.

The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network composed of quantum logic gates or circuits; each gate performs an elementary unitary operation on one, two or more two state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. The quantum networks cannot be directly deduced from their classical Boolean counterparts which are clearly irreversible. Thus, quantum arithmetic must be built from reversible logic components [5]. The reversible logic gate or circuit is a n-input n-output logic function in which there is a one-to-one correspondence between the inputs and the outputs. Because of this bijective mapping the input vector can be uniquely determined from the output vector. This prevents the loss of information which is the root cause of power dissipation in irreversible logic circuits. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits [6, 4 and 7].They are listed below.

The number of Reversible gates (N): The number of reversible gates used in circuit. The number of constant inputs (CI): This refers to the number of inputs that are to be maintained either at 0 or 1 in order to synthesize the given logical function. The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit.

2.2. Important reversible logic gates

Feynman gate [7, 8], and BVF gate [9] are the two reversible logic gates used in this work, along with the MTG.

1) Feynman / CNOT Gate (FG): Fig 1. shows the Feynman gate which is a 2*2 gate and is also called as Controlled NOT and it is widely used for fan-out purposes. The inputs (A, B) and outputs P=A, Q= A⊚ B. It's Quantum cost is one.

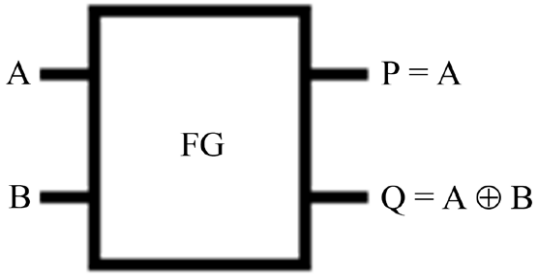

Fig 1. Feynman gate

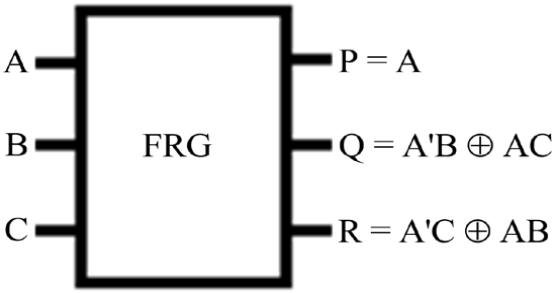

Fig 2. Fredkin gate

This is a (4, 4) reversible logic gate [13] shown in Figure 6 with input vector I (A, B, C, D) and the output vector is O (P, Q, R, S) .

3. PROPOSED QUANTUM REALIZATION OF MTG (MODIFIED TOFFOLI GATE)

The proposed quantum realization of this gate is shown in fig 3.. The MTG is designed from two controlled V gate and two CNOT gate resulting in quantum cost of 5. Further logic depth of quantum implementation of MTG is 5. This results in propagation delay as 5 Δ, where Δ is the unit delay. Table 1 shows the truth table of MTG. This paper presents a new (3, 3) reversible gate, "DG"

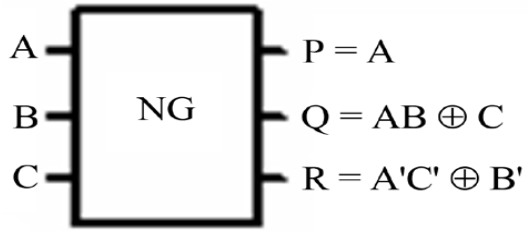

Fig 3. New gate

Applications of MTG

MTG can be used for the following applications.
1. Fan-out
2. Logical operations
3. Arithmetic operations

1) MTG can be used for fan-out purpose by applying constant inputs at its inputs which is summarized as shown in the table.2

TABLE 1 MTG AS A FAN-OUT GATE

A	B	C	P	Q	R
A	0	0	A	0	A
0	B	0	0	B	B

3.1 Implementation of One-bit Irreversible Comparator

The conventional one-bit irreversible numerical comparator, which consists of two NOT gates, two AND gates and one NOR gate [10], is shown in Fig.3a with its truth table in Table 2. We can get the following logic expressions from Table 2.

$$\begin{cases} F_{A>B} = A\overline{B} \\ F_{A<B} = \overline{A}B \\ F_{A=B} = \overline{A \oplus B} \end{cases}$$

Table 2. Truth table of 1- bit comparator

Input		Output		
A	*B*	$F_{A>B}$	$F_{A<B}$	$F_{A=B}$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

It is observed from the above table that, if any two conditions are not satisfied, it is understood that the third condition will be true. So one of the outputs can be generated from the remaining two outputs and thus the design can be optimized. In the proposed one-bit comparator [11] design, we have considered FA>B and FA=B and the third condition FA<B is generated from the first two outputs.

$$\begin{cases} F_{A>B} = A\overline{B} \\ F_{A=B} = \overline{A \oplus B} \\ F_{A<B} = \overline{(\overline{A \oplus B})} \cdot \overline{(A\overline{B})} \end{cases}$$

This design requires one NOT gate, one AND gate and one ENOR (Ex-Nor) gate and one NOR gate.

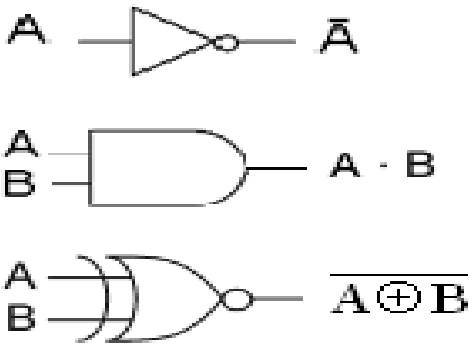

Fig.4 . Irreversible gates for Numerical comparator

3.2 The proposed one bit Reversible comparator designs

All the gates mentioned in section 2 can be used for the construction of reversible comparators. Here the proposed BJN gate is used in the last stage of comparator to generate all the outputs of comparator. Using this gate in combination with existing reversible gates, garbage output, quantum cost[12] and gate counts are reduced.

3.2.1. One- bit comparator using Peres and BJN gate

one bit comparator is implemented with Feynman gate and Peres gate and BJN gate as shown in fig.5. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs one logic '0' and two logic '1'.

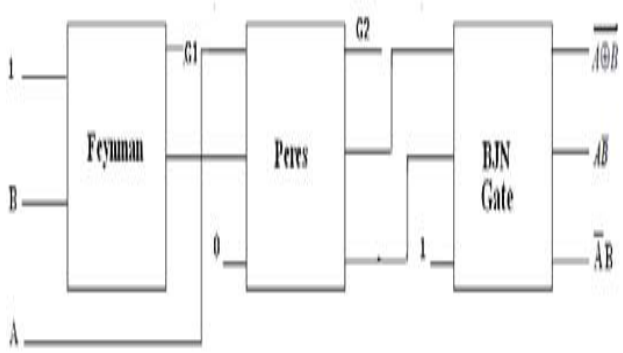

Fig.5. one bit comparator using Peres gate

3.2.2. One bit comparator using Toffoli and BJN gate

Reversible one bit comparator is implemented with Feynman gate[14] and Toffoli gate as shown in fig.6. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs , one logic '0' and two logic '1' it requires one Feynman gate and two Toffoli gates.

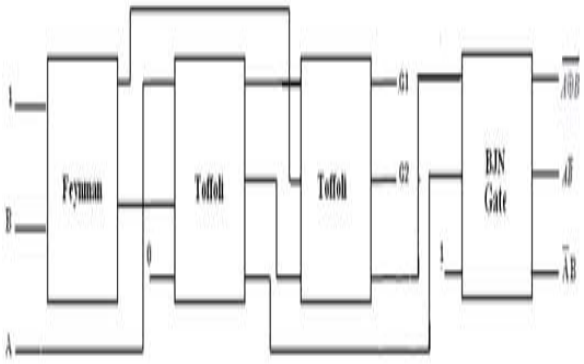

Fig. 6. One bit comparator using Toffoli gate

3.2.3. one bit comparator using R and BJN gate

Reversible one bit comparator is implemented with Feynman gate and R gate as shown in fig.7. The number of garbage outputs is two and represented as G1, it uses two constant logic '1' input. It requires one Feynman
gate and one R gate.

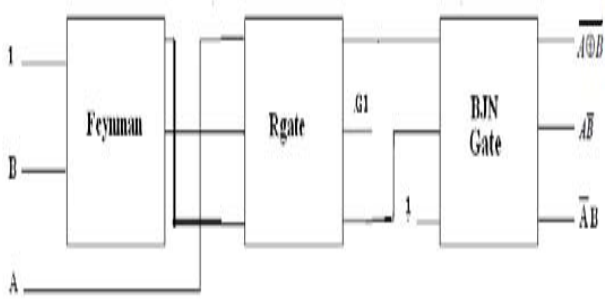

Fig.7. one bit comparator using R gate

3.2.4. one bit comparator using TR and BJN gate

Reversible one bit comparator is implemented with Feynman gate and TR gate and BJN gate as shown in fig.8. The number of garbage outputs are two and represented with G1 and G2, it uses three constant inputs, one logic '0' and two logic '1'.

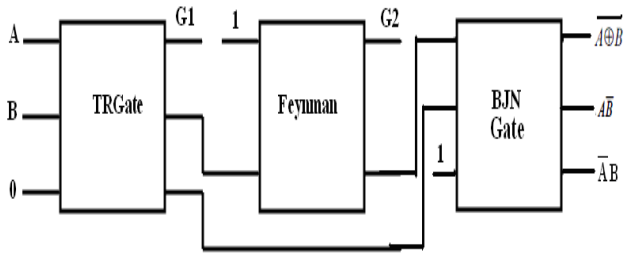

Fig. 8. one bit comparator using TR gate

4. SIMULATION RESULTS

Reversible logic gates are extensively known to be compatible with future computing technologies which approximately dissipate zero heat [15]. For example, Reversible three bit comparators offered using VHDL and Simulated using Quartus II Simulator.

Garbage Outputs: This refers to the number of outputs which are not used in the synthesis of a given function. These are very essential without which reversibility cannot be achieved.

Gate count: The number of reversible gates used to realize the function.

Constant Inputs: This refers to the constant inputs '0' or '1'.

From the comparison results of all comparator designs shown in table3 and chart 1 , it is compared in terms of gate count, Garbage output and number of constant inputs. It is evident from the results from Peres with BJN is optimized design in comparison with other designs. The proposed designs were functionally verified through simulations coding their designs in the Verilog Hardware Description Language[15]. In order to achieve this, we built a library of reversible gates in Verilog HDL and use it to code the proposed designs of sequential circuits. The library contains the Verilog codes of reversible gates such as the Fredkin gate, the Toffoli gate, the Peres gate, etc. We have created test benches for every reversible sequential circuits proposed in this work to verify their correctness.

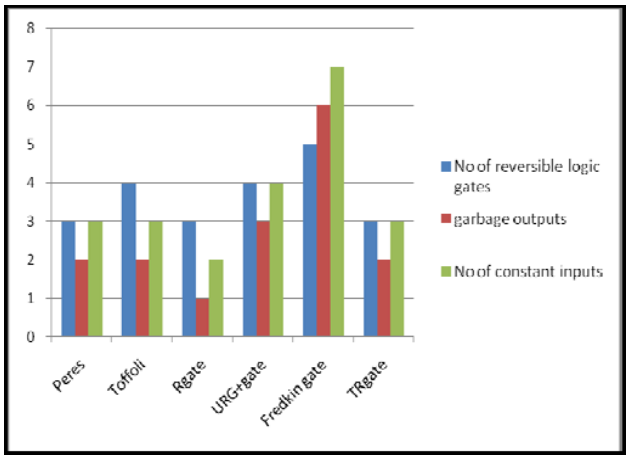

Chart 1. Comparison Results

5. CONCLUSION

In this paper an optimized reversible comparator is presented with the proposed new Reversible BJN gate. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of number of reversible logic gates, number of garbage outputs and number of constant inputs. The analysis of various implementations discussed are tabulated in Table2.It gives the comparisons of the different designs in terms of the important design parameters like number of reversible gates, number of garbage outputs and number of constant inputs and quantum cost. The performance parameters are optimized in comparison with the existing numerical comparator.

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