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Design of an efficient aging aware reliable multiplier to reduce aging effects

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Abstract:-Digital multipliers are among the most critical arithmetic functional units. The Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed.. There are three types of multipliers Vedic multiplier base on Vedic arithmetic using Urdhva-Tiryabhyam sutra are proved to be the most efficient in terms of lower power consumption. overall performance of these systems depends on the throughput of the multiplier .A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. A multiplier is one of the chief hardware blocks in most digital and high concert systems such as microprocessors, digital signal processors. The CNFET-based multipliers have higher speed, and low power dissipation and it nearly reduces 99% PDP (power-delay product) as compared to the MOSFET In this paper, we propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. The experimental results show that our proposed architecture with 16 ×16 and 32 ×32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column-bypassing multipliers

Keywords –Adaptive Hold Logic(AHL), variable Latency, Reliable Multiplier, Positive Bias Temperature Instability(PBTI),Negative Bias Temperature Instability(PBTI)

1 .INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage, reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. The throughput of these applications depends on multipliers, and if The multipliers are too slow, the performance of entire circuits will be reduced. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors, and therefore is usually ignored. A traditional method to mitigate the aging effect is overdesign [1] including such things as guard-banding and gate oversizing however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI-aware methodologies have been proposed. An NBTI-aware technology mapping technique was proposed in to guarantee the performance of the circuit during its lifetime. In [2], an NBTI-aware sleep transistor was designed to reduce the aging effects on pMOS sleep-transistors, and the lifetime stability of the power-gated circuits under consideration was improved.Wu and Marculescu [2] proposed a joint logic restructuring and

pin reordering method, which is based on detecting functional symmetries and transistor stacking effects. They also proposed an NBTI optimization method that considered path sensitization. In [3] and [4], dynamic voltage scaling and body-basing techniques were proposed to reduce power or extend circuit life. These techniques, however, require circuit modification or do not provide optimization of specific circuits. The first array multiplier is designed but it has more digital logic gates and consumes higher power [4].So to overcome this issues Wallace multiplier is designed and it is faster than a simple array multiplier because of its non linearity but Wallace trees are often avoided by designers and compare to other multiplier like array, the Wallace multiplier Vedic multiplier is quicker and consumes lesser power. Power conservation is a key concern in the VLSI circuit design so here low power technique Multi-Threshold Voltage CMOS (MTCMOS) is applied so efficient power management is achieve. In this paper, analysis and comparison of multipliers using different design techniques are performed. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. However, the probability that the critical paths are activated is low. In most cases, the path delay is shorter than the critical path. For these noncritical paths, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable-latency design was proposed to reduce the timing waste of traditional circuits.

The variable-latency design divides the circuit into two parts: 1) shorter paths and 2) longer paths. Shorter paths can execute correctly in one cycle, whereas longer paths need two cycles to execute. When shorter paths are activated frequently, the average latency of variable-latency designs is better than that of traditional designs. For example, several variable-latency adders were proposed using the speculation technique with error detection and recovery.

A short path activation function algorithm was proposed in to improve the accuracy of the hold logic and to optimize the performance of the variable-latency circuit. An instruction scheduling algorithm was proposed in to schedule the operations on non-uniform latency functional units and improve the performance of Very Long Instruction Word processors. In a variable-latency pipelined multiplier architecture with a Booth algorithm was proposed.

In process-variation tolerant architecture for arithmetic units was proposed, where the effect of process-variation is considered to increase the circuit yield. In addition, the critical paths are divided into two shorter paths that could be unequal and the clock cycle is set to the delay of the longer one. These research designs were able to reduce the timing waste of traditional circuits to improve performance, but they did not consider the aging effect and could not adjust themselves during the runtime. A variable- latency [5] adder design that considers the aging effect was proposed. However, no variable-latency multiplier design that considers the aging effect and can adjust dynamically has been done. Compared to silicon technology, CNFET shows improved device performance (based on the intrinsic CV/I gate delay metric (6× for nFET and 14× for pFET) than a MOSFET[5] device at the 32 nm node, with device non-idealities. This outsized speed improvement is extensively degraded (~5× degradation) by interlock capacitance in a real circuit environment. Growing the number of CNTs per device is the most valuable way to progress the circuit speed.

2 .PRELIMINARIES

2.1 Column-Bypassing Multiplier

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 1. The multiplier array consists of (n − 1) rows of carry save adder (CSA), in which each row contains (n − 1) full adder (FA) cells.

Each FA in the CSA array has two outputs:

1) The sum bit goes down
2) The carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation.

The FAs in the AM are always active regardless of input states. In [6], a low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 1 shows a 4 × 4 column-bypassing multiplier. The multiplicand bit can be used as the selector of the multiplexer to decide the output of the FA, and ai can also be used as the selector of the tri state gate to turn off the input path of the FA.

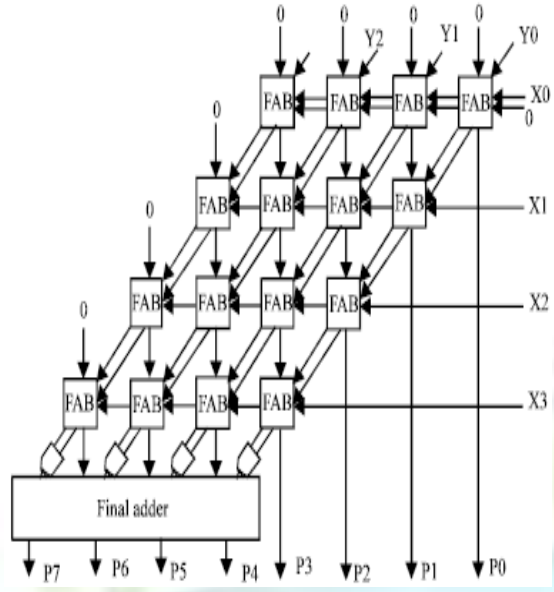


Fig.1 4 × 4 Column by Passing Multiplier

2.2 Row-Bypassing Multiplier

A low-power row-bypassing multiplier [7] is also proposed to reduce the activity power of the Array Multiplier. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing multiplier, but the selector of the multiplexers and the tristate gates use the multiplicator. Fig. 2 is a 4 × 4 row-bypassing multiplier. Each input is connected to an FA through a tristate gate. When the inputs are 11112 * 10012, the two inputs in the first and second rows are 0 for FAs. Because b1 is 0, the multiplexers in the first row select ai b0 as the sum bit and select 0 as the carry bit. The inputs are by passed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similarly, because b2 is 0, no switching activities will occur in the second-row FAs

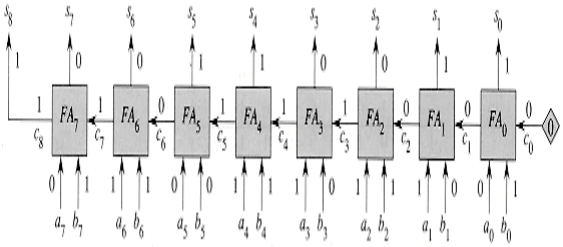


Fig. 2 Row by Passing Multiplier

2.3 Aging Model

When the bias voltage is removed, the recovery process occurs, reducing the drift. If a pMOS (nMOS) transistor is under constant stress, this is referred to as static NBTI (PBTI). If both stress and recovery phases exist, it is referred to as dynamic NBTI (PBTI). The drift of pMOS (nMOS) transistor due to the static NBTI (PBTI) effect can be described by dc reaction-diffusion (RD) framework. If transistors are under alternative stress and recovery phases, the dc RD model should be modified to an ac RD model [8], where α is a function of stress frequency and signal probability (S). Since the impact of frequency is relatively insignificant, the effect of signal frequency is ignored. KDC is a technology-dependent constant where A is a constant, and TOX is the oxide thickness.

EOX is the gate electric field, which the Boltzmann constant, and T is the temperature. E0 and Ea are technology-independent characteristics of the reaction that are equal to 1.9–2.0 MV/cm and 0.12, respectively. We use 32-nm high-k metal gate models. We set the temperature at 125 °C in our simulation and use the above BTI model to predict the BTI effect on the circuits. Fig. 2 shows the simulated delays of the 16 × 16 column-and row-bypassing multipliers under a seven-year NBTI/PBTI effect. From this figure, it can be seen that the BTI effect increased the critical path circuit delay by 13%. Hence, if the BTI effect is not considered during circuit design, the increased delay may cause system failure in the long term.

3 .PROPOSED AGING-AWARE MULTIPLIER

The proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs. Our proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops [9], and an AHL circuit. In the proposed architecture, the column- and row-bypassing multipliers can be examined by the number of zeros in either the multiplicand or multiplicator to predict whether the operation requires one cycle or two cycles to complete.

3.1 Proposed Architecture

proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops[10], and an AHL circuit. Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the column or row-bypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing multiplier [15] is the multiplicand, whereas of the row-bypassing multiplier is the multiplicator.

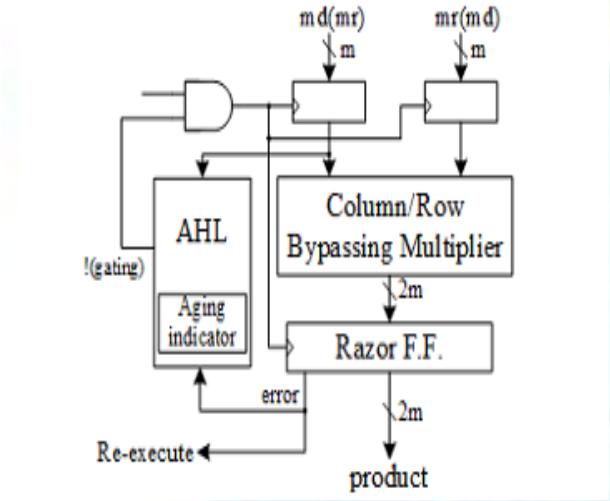


Fig 3. Architecture of AHL (md means multiplicand; mr Means multiplicator).

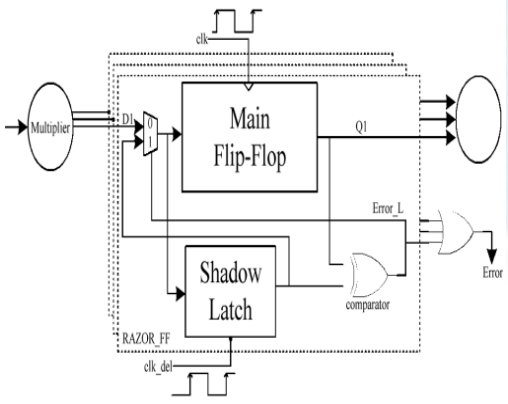
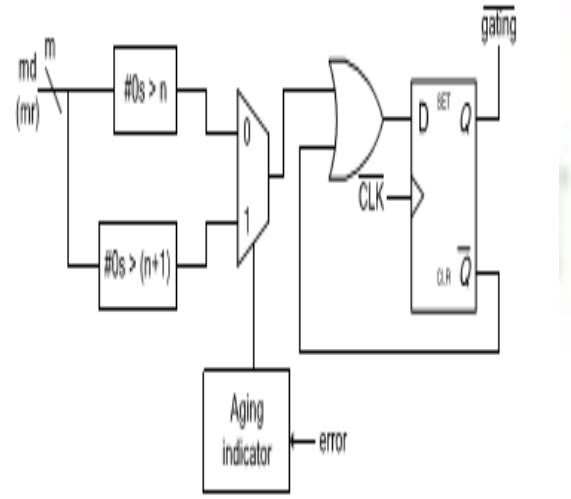


Fig 4. Internal Block Diagram of Razor flip flop.

Razor flip-flops can be used to detect. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop[14] catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. To notify the system to re-execute the operation and notify the AHL circuit that an error has occurred. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the razor flip-flop will set the error signal to 1.



Fig, 5 Diagram of Adaptive Hold Logic

Although the re execution may seem costly, the overall cost is low because the reexecution frequency is low. More details for the Razor flip-flop can be found [11]. The AHL circuit is the key component in the aging-ware variable-latency multiplier. Fig .5 shows the details of the AHL circuit. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect. The aging indicator is implemented in a simple counter that counts the number of errors over a certain amount of operations and is reset to zero at the end of those operations.

4. MTCMOS TECHNIQUE

Power consumption is a major concern in the VLSI circuit design, high power consumption leads to reduction in battery life like movable phones, laptops etc. and affects the reliability of the system. To employ long standby periods by dropping the leakage current is highly significant to provide longevity for the succession.

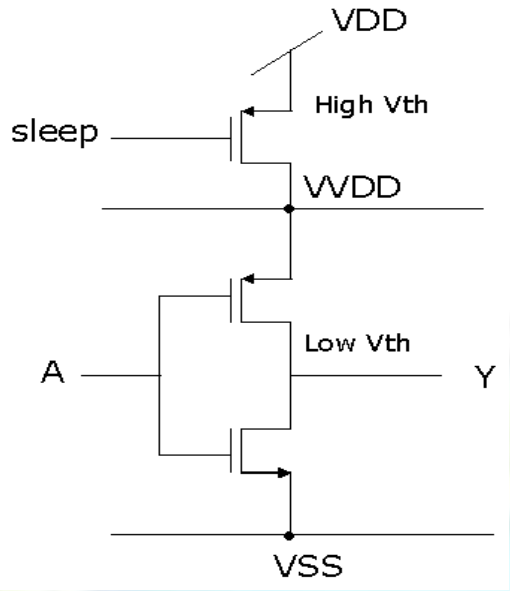


Fig.6 Power gating transistor

The extremely suggested circuit technique for the outflow current decline is the Multi-Threshold Voltage CMOS (MTCMOS). In MTCMOS technology, capable power managing is obtained by allowing the circuit to function in two modes: 1) energetic Mode 2) Sleep Mode. The power gating technique is one kind of multi-threshold voltage CMOS (MTCMOS) technique[12] where a sleep transistor[13] is added between control supply and ground it turns off the plans by cutting off their supply voltage. This method uses further transistors (sleep), which are inserted in the chain between the power supply and pull-up network (PMOS) and/or between pull-down (NMOS) network and ground to cut the standby leakage currents. The sleep transistors are turned on when the circuit are in energetic mode and turned off when circuits are in standby mode.

5. COMPARISON AND SIMULATION RESULTS.

Implementation of 4x4 as well as 8x8 bit three different types of multipliers using MOSFET, CNFET, and using MTCMOS technique using 32nm the Berkeley Predictive Technology Model (BPTM) has been carried out on H-spice tool. Power consumption and Power Delay Product (PDP) comparisons for 4x4 as well as 8x8 bit for three different types of multipliers i.e. Array multiplier, Wallace multiplier, Vedic multipliers are stimulated at 1v voltage. Here the comparison of multipliers is made between MOSFET AND CNFET 32nm technologies.

Table 1: Analysis of 4*4 Multipliers cell between MOSFET 32nm and CNTFET 32nm technology

4 × 4 Multipliers	MOSFET 32nm Power delay Product (w/s)	CNTFET 32nm Power delay Product (w/s)
Array Multiplier	2.7784E-15	6.9754E-18
Wallace Multiplier	1.0828E-15	2.7769E-18
Vedic Multiplier	5.6090E-16	1.6694E-18

Table 2: Analysis of 8*8 Multipliers cell between MOSFET 32nm and CNTFET 32nm technology

8 × 8 Multipliers	MOSFET 32nm Power delay Product (w/s)	CNTFET 32nm Power delay Product (w/s)
Array Multiplier	1.4363E-13	5.7745E-15
Wallace Multiplier	1.6161E-14	3.5517E-17
Vedic Multiplier	4.8615E-15	1.2926E-17

6. CONCLUSION

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. THE multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The multiplier is based on the variable-latency with razor flip flop technique. The efficiency of the proposed architecture will be increased. Our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste. The AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. Our proposed architecture with the 16×16 column-bypassing multipliers and row-bypassing multipliers. A comparative study was also

done between Vedic multiplier without using AHL and using AHL. It was inferred that the power and delay got reduced while using 4x4vedic multiplier with AHL.

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